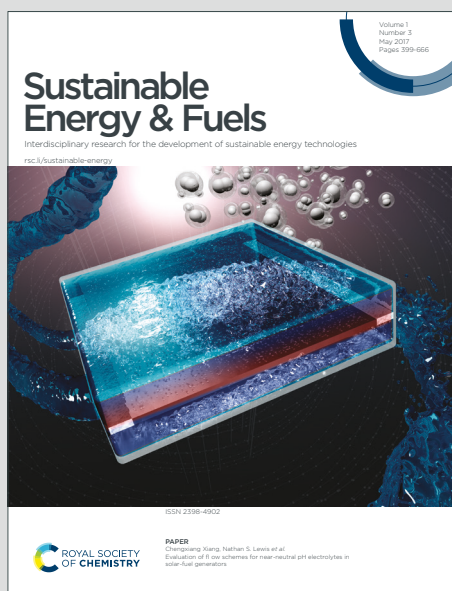


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# Perceiving the Temperature Coefficients of Carbon-based Perovskite Solar Cells

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DOI: 10.1039/D0SE00782J

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## Abstract

Perovskite solar cells (PSCs) have emerged in a "catfish effect" of other established photovoltaic technologies with the rapid development of high-power conversion efficiency (PCE) and low-cost fabrication. Among various kinds of PSCs, the organic hole transport layer (HTL) free carbon-based PSCs (c-PSCs) has appeared as the most promising devices due to its excellent stability. However, temperature becomes one of the crucial factors in determining the pace of PSCs commercialization. Temperature stress at the interfaces between the perovskite film and the charge transport layers is an essential factor in determining the performance of c-PSCs. This work assesses the correlation between the temperature coefficients ( $T_C$ ) and different photovoltaic parameters for HTL free c-PSCs. To evaluate different photovoltaic parameters of the c-PSC as a function of temperature, two different testing approaches such as steady temperature ( $S_T$ ) and transient temperature ( $T_T$ ) conditions have been considered across a wide range of temperature window (5–75 °C) under 1 SUN 1.5 AM. Here the  $T_T$  testing stands for a single c-PSC undergoing a continuous temperature treatment whereas; the  $S_T$  testing indicates specific temperature treatment for an individual c-PSC. The maximum efficiency achieved at 25 °C for  $T_T$  testing devices is ~14.5%, which is ~11% higher than the  $S_T$  testing devices (PCE ~13%). Moreover, the efficiency temperature coefficient (ETC) for  $S_T$  testing was found  $3.5 \times 10^{-2}$  (5 °C  $\leq T \leq 25$  °C) and  $-2.1 \times 10^{-2}$  (25 °C  $\leq T \leq 75$  °C), whereas the ETC values of  $T_T$  testing devices were  $+2.5 \times 10^{-2}$  (5 °C  $\leq T \leq 25$  °C) and  $-1.8 \times 10^{-2}$  (25 °C  $\leq T \leq 75$  °C), respectively. The outcome of the temperature stress transmitting through different interfacial layers was further investigated by the thermal imaging for  $T_T$  devices. On the other hand, X-ray diffraction and scanning electron microscope structural analysis were demonstrated to understand the thermal stress on the overall performance of  $S_T$  devices. It has been observed that the  $T_C$  values resulting from  $T_T$  testing condition are reversible, whereas in the case of  $S_T$  testing shows irreversible nature and facilitates degradation of the device.



## Introduction

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Perovskite solar cells (PSCs) with its cutting-edge technology, has been universally elevated as an economically and environmentally feasible renewable technology option in place of regular and traditional solar cell technologies for addressing the global challenges in the area of energy generation and climate change.<sup>1,2</sup> From initial development to use of carbon as a counter electrode, extensive works have been done in this field, and till date, PSC achieved highest photo-conversion efficiency (PCE) of 25.2%.<sup>3–19</sup> Seeking for interfacial engineering and the grain boundary in the perovskite layer insight can further help to integrate the PSC field towards more stable, reliable and enhanced PCE generating devices. Instead of this massive development, there are issues like upscaling, toxicity, and stability of performance that binds PSCs from commercialization.<sup>2,20</sup> Due to the cost-effectiveness, environmental superiority, abundant, and excellent photo-electrochemical catalytic activity, carbon plays critical roles in the charge transport layer, as well as the counter electrode utilizing different polymorphs like carbon nanotube, fullerene, graphite, graphene.<sup>21–23</sup> Carbon polymorphs as charge transport material, produced the highest PCE of 21.1% whereas as electrode material for hole-selective layer free devices, it was able to provide the highest PCE of 16.26%.<sup>24,25</sup> With the potential of achieving even higher efficiencies and very low production costs, c-PSCs have become commercially attractive.

However, the temperature is one of the most crucial outdoor variables that influence the photovoltaic performance and stability of the PSCs. Temperature strongly influences physical parameters, like the charge diffusion in the layers and/or recombination reactions of the generated electrons in the device.<sup>26</sup> To the date, studies on temperature-dependent c-PSCs are the limited and less-explored area of research compared with the numerous studies on improving the PCE and stability of the c-PSC devices. There are few studies on temperature-dependent PSC, which suggests a maximum PCE around room temperature with the successive performance curtailment at a higher or lower temperature condition.<sup>27–30</sup> Most of the studies reveal the accumulation of ions in selective interfacial contacts during temperature stress. This is further signifying evaporation of additives in the hole transport layer (HTL) as the reason behind such performance decline of a PSC device.<sup>31,32</sup> In this regard, our study aims to investigate and understand the role of temperature coefficients ( $T_C$ ) of c-PSCs as obtained from the photovoltaic parameters such as short circuit current ( $J_{SC}$ ), open-circuit voltage ( $V_{OC}$ ), fill factor (FF) and power conversion efficiency (PCE) in visualizing the marketing of solar cells.<sup>33,34</sup> The relative change of a temperature-dependent parameter corresponding to the



change of temperature is known as the temperature coefficient of that parameter.<sup>35</sup> The physics of temperature coefficients ( $T_C$ ) of solar cell suggests a strong dependency of  $V_{OC}$  and  $J_{SC}$  on the temperature, as the balance between charge carrier generation and recombination can be affected by temperature.<sup>34</sup> Also, the temperature dependency of bandgap shift plays a vital role along with the incident spectrum to affect the cell parameters.<sup>36</sup> Extensive research on performance variation with temperature to pin-point temperature coefficient and deducing origin of interfacial damages needs unfolding for c-PSCs. It has been observed that the three most widely commercialized thin-film solar cells such as  $\alpha$ -Si, CdTe and copper indium gallium selenide, the  $T_C$  value is negative.<sup>37,38</sup> Although, they are highly effective in large scale operation. Negative  $T_C$  value normally implies that with the increase of temperature, the parameter of interest will decrease, which can affect the performance of solar cell in a hot climate. Again a positive  $T_C$  value indicates that the increase of temperature will increase the performance, which can impact the performance of the device at cold climate.<sup>39</sup> In contrast, reports on  $T_C$  values evaluation is less explored for PSCs. The marketization of PSCs highly depends on the  $T_C$  value of the devices because PV cells in the ground are operated at lower or higher temperatures relative to standard test condition (STC, the temperature is taken as 25 °C), depending on the environment, leading to changes in the average PCE, as reported for silicon solar cells.<sup>33,34,40–43</sup> At different climatic condition, the yearly average temperature varies significantly from the STC.<sup>44</sup> On the earth surface; every location usually undergoes a daily (in 24 hours) temperature variation of ~5 to 10 °C or sometimes more than that.<sup>45,46</sup> In areas where the variation is ~5 °C or less in 24 hours, it is possible that the performance of the devices can be different from places where the variation is 10 °C or more due to inherent properties of materials like specific heat capacities.<sup>47,48</sup> A change of 10 °C can significantly vary the performance of PSC devices, and detection of  $T_C$  value is inevitable in this scenario. This kind of temperature variation can disrupt the instantaneous thermal equilibrium between different materials depending on specific heat capacity and thermal conductivity.<sup>49</sup> Therefore, in this work, the steady temperature ( $S_T$ ) and transient temperature ( $T_T$ ) temperature conditions are introduced to understand its effect on the interfaces between the  $CH_3NH_3PbI_3$  perovskite film and the charge transport layers and on the performances of c-PSCs in the temperature range of 5 °C to 75 °C. Here  $S_T$  and  $T_T$  terms are designated depending on conditions of experimentation. A particular device characterized at different temperatures starting from 5 °C to 75 °C is termed as  $T_T$  testing, which could be more realistic for everyday temperature variation of  $\geq 10$  °C on the earth surface. On the other hand, different devices kept

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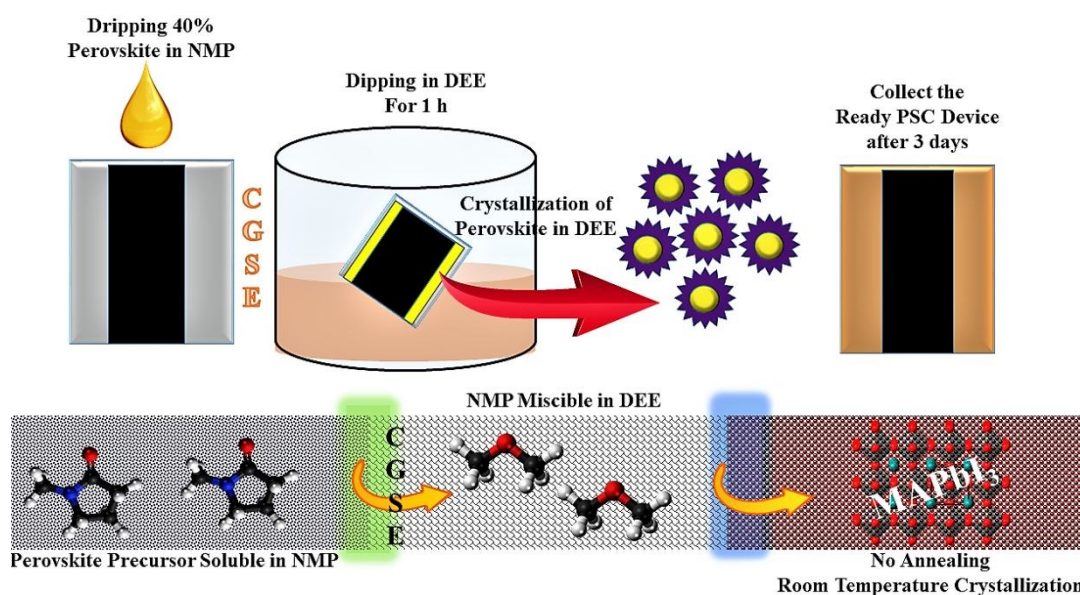


at different temperatures (i.e. a particular device was kept at a particular temperature) in 5 °C to 75 °C range for examination is called as  $S_T$  testing, which could be more realistic for everyday temperature variation  $\leq 5$  °C for a long time. Observations indicate a clear spectrum of  $T_C$  values of different photovoltaic parameters for the first time, along with the probable reasons behind significant performance variations. This finding will be relevant for industrial applications in both single-junction and tandem architectures for the c-PSC devices in future.

## Results and Discussion

### Crystal growth via solvent exchange method to develop c-PSC

Crystal growth via solvent exchange (CGSE) method turns out as an effective one-step approach for the fabrication of organic hole-conductor free carbon-based perovskite solar cells with superior device performance.<sup>50</sup> At the same time, it allows the room-temperature solution processing fabrication method to develop crystalline, scalable and rapid perovskite thin films with no further heat-treatment. The investigated unencapsulated c-PSCs had the conventional n-i-p structure of FTO/ Compact  $\text{TiO}_2$ / mesoporous  $\text{TiO}_2$ / mesoporous  $\text{Al}_2\text{O}_3$ /  $\text{WO}_3$  incorporated carbon.  $\text{MAPbI}_3$  precursor solution was drop-casted and spin-coated from the top of the counter electrode. Crystal growth via solvent exchange (CGSE) was then applied for room-temperature deposition of perovskite thin film, as shown in Fig. 1. The details of the device fabrication process have been described in the experimental section.

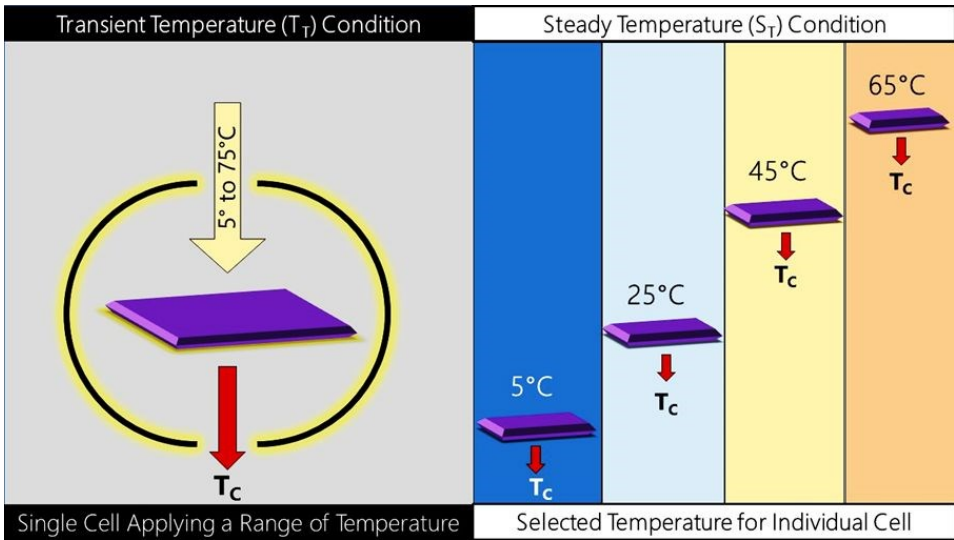




**Fig. 1** Schematic illustration showing the CGSE process for the room- temperature deposition of MAPbI<sub>3</sub> thin film to fabricate c-PSC. The process of perovskite formation without any heat treatment was performed for three days for fine crystallization. Exchange of N-methyl-2-pyrrolidone (NMP) with Diethyl ether (DEE) helped in the formation of pure crystal phase (the yellow arrows represent the crystal growth process by changing the solvent medium).

**Testing approaches to determine the temperature coefficients ( $T_C$ )**

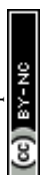
In order to find out the  $T_C$  values, the fabricated devices were employed for two different testing conditions such as  $S_T$  and  $T_T$ . The  $S_T$  testing devices were placed at a particular temperature for 2 days before any further characterization. For example, at low temperature like 5 °C, it was kept in a chamber where the surrounding temperature was 5 °C and similarly for other temperatures without interfering with factors like moisture and air. In contrast, for the  $T_T$  testing, a single device was placed at each particular temperature using covered vacuum temperature controller to maintain surrounding temperature (system under vacuum to avoid air and condensation) for ~1 hour (~30 mins to reach the required temperature and then kept at that temperature for ~30 mins) for performance evaluation. A schematic of the testing details has been given in Fig. 2.



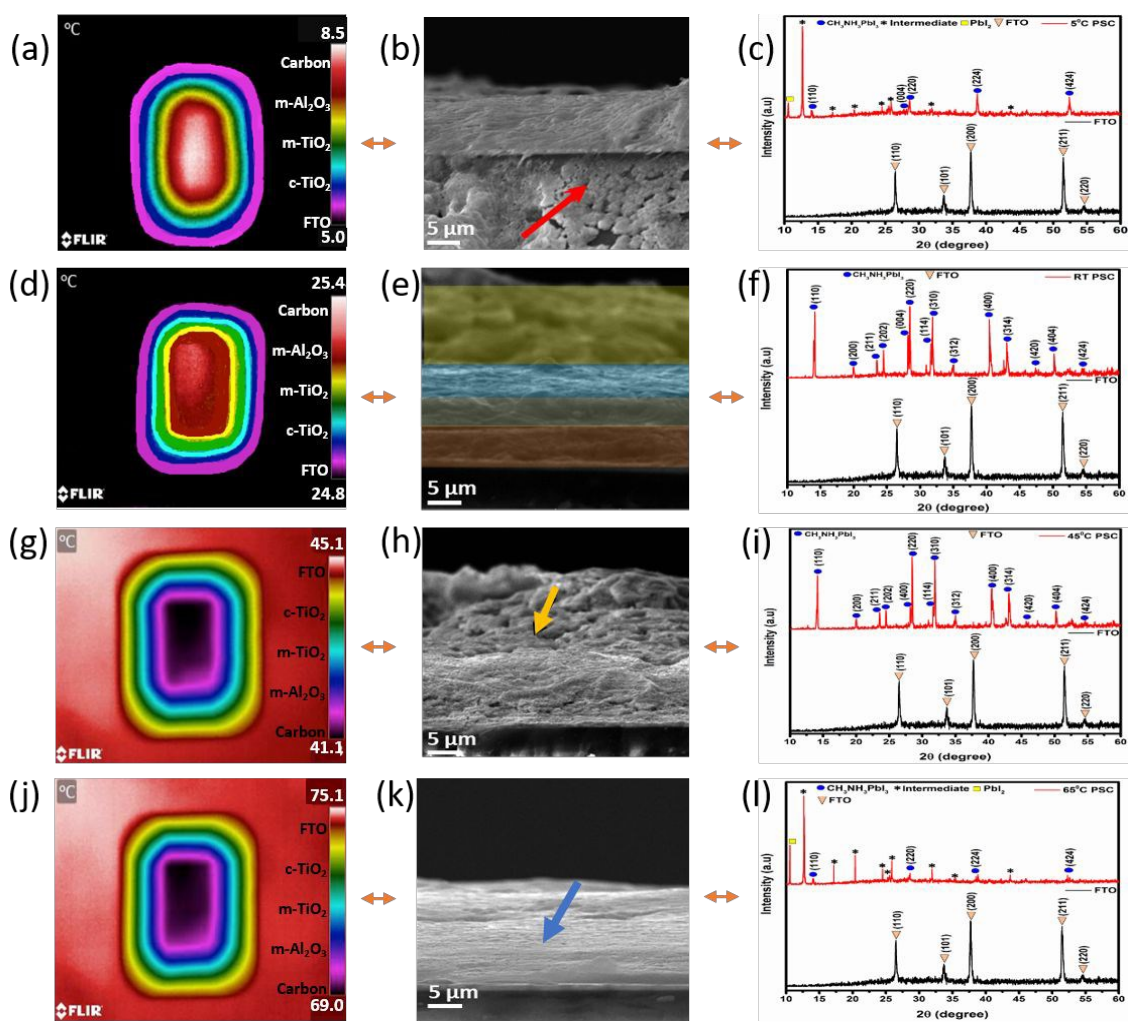
**Fig. 2** Schematic of two different pathways of testing named as transient temperature test ( $T_T$ ) and steady temperature test ( $S_T$ ).

**Thermal, X-ray diffraction and microstructural analysis of c-PSCs**

The  $S_T$  devices were further investigated using scanning electron microscopy (SEM) and powder X-ray diffraction (XRD) characterizations. In contrast, thermal imaging was introduced to characterize the devices under  $T_T$  testing conditions. The SEM and XRD pattern of the fabricated c-PSCs at four different  $S_T$  testing conditions such as 5 °C, 25 °C, 45 °C and 65 °C, respectively, are shown in Fig. 3, where significant changes have been observed for different interfacial layers associated in the PSC device.  $S_T$  devices were maintained at a particular temperature for two days before executing the respective characterizations. For thermal images, as shown in Fig. 3, the  $T_T$  testing devices were prepared as follows. At first c-TiO<sub>2</sub> layer was deposited over the entire fluorine-doped tin oxide (FTO) coated glass surface, and after sintering and cooling, this layer was taped from every side to reduce the surface aperture area of the next layer. In this way, successively the surface aperture area of every layer was reduced from its preceding ones to monitor the thermal imaging of the individual layer. After that, the devices were kept at a particular temperature with a covered vacuum temperature controller to maintain a similar temperature surrounding the device. Starting from the ambient condition, for each set of temperature, 30 min was allowed to attain the set temperature, and then it was kept for ~30 mins in order to capture the thermal images. This is how top surface thermal images can spot different layers separately to perceive the temperature profile of the layers. Usually, the environment temperature is variable (may be minor) throughout the day, which should affect the instantaneous thermal equilibrium of different materials due to their inherent properties. Similarly, the thermal images captured for c-PSC can predominately correlate with outdoor circumstances where different layers could not be in instantaneous thermal equilibrium all the time. Fundamentally, different materials have different heat capacities which will effectively take part to disrupt the thermal equilibrium of different layers of real-world PSC devices. Thermal images at a specific temperature exhibit the nature of interfacial layers under different temperature stress. At a lower temperature, the FTO layer maintains 5 °C, whereas the compact-TiO<sub>2</sub> layer remains at around 5.7 °C. On the other hand, m-TiO<sub>2</sub> and m-Al<sub>2</sub>O<sub>3</sub> layers maintain a temperature of 6.2 °C and 7 °C, respectively. The carbon layer confines the maximum amount of temperature, which is reflected from thermal images of around 8.5 °C. It can be predicted that the temperature difference of m-TiO<sub>2</sub>, m-Al<sub>2</sub>O<sub>3</sub> and carbon layer can promote the ion migration at this low-temperature region relative to a system in equilibrium.<sup>29</sup> In this scenario, analysing the SEM and XRD of the devices kept at 5 °C can clarify  $S_T$  behaviour. XRD data suggests the formation of PbI<sub>2</sub> and some other intermediate at ~ 5 °C. The degradation from CH<sub>3</sub>NH<sub>3</sub>PbI<sub>3</sub> (MAPbI<sub>3</sub>) to PbI<sub>2</sub> is most likely accompanied by a chemical reaction under thermal stress.<sup>51</sup> On the other hand, SEM points



towards spill-over of  $\text{PbI}_2$  through  $\text{m-TiO}_2$  and  $\text{m-Al}_2\text{O}_3$  layers, as shown by the arrow in Fig. 3b. The spill-over is only possible due to *in-situ* layer formation at the interfaces of the deposited layers, causing unrecognizable layer separations in the device architecture (Fig. 3b). In Fig. 3c, the XRD analysis also suggests the formation of  $\text{PbI}_2$ , which triggers the spill-over, leading to affect the photovoltaic performances of devices to a great extent. At 25 °C, the separated layers of the c-PSC are quite distinct, as shown in Fig. 3d-f. Prominent layer distinction was also observed in SEM, as shown with colours in Fig. 3e and also the XRD data suggests the formation of stable perovskite having major peaks at 14.10°, 23.47°, 28.42°, and 30.89° corresponding to the (110), (211), (220), (310) planes of  $\text{CH}_3\text{NH}_3\text{PbI}_3$ , respectively. Interestingly, at 25°C, the corresponding thermal image (Fig. 3d) exhibits insignificant variation among the layers. It has also been suggested that the small amount of excess  $\text{PbI}_2$  in perovskite influences on the morphology and increases the size as well as uniformity of perovskite crystals by solvent engineering method.<sup>52</sup>



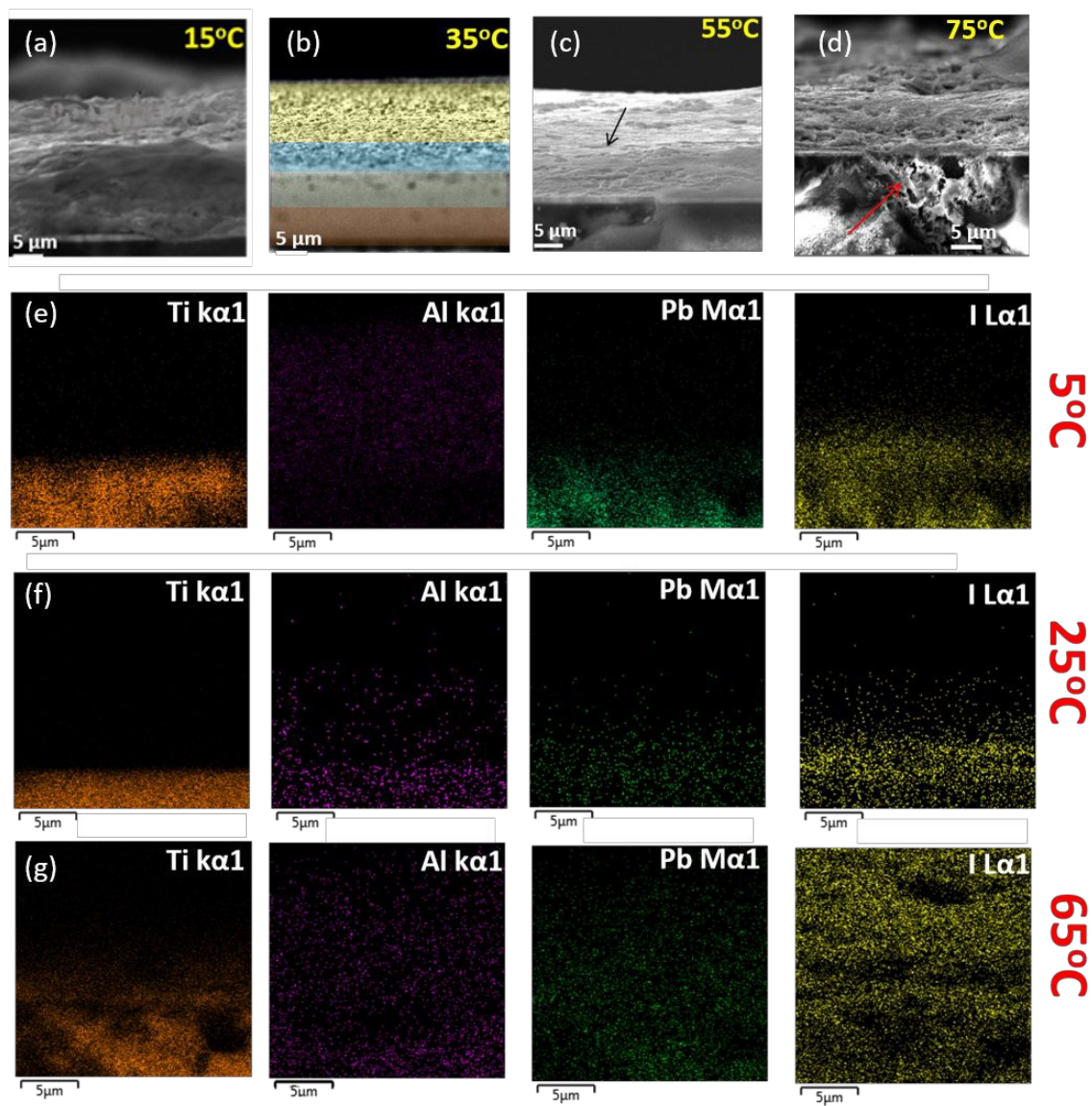


**Fig. 3** (a), (b), and (c) are the top surface thermal image of  $T_T$  device, SEM, and XRD at 5 °C for  $S_T$  cases, respectively (arrow in SEM suggests the formation of intermediate and exfoliation of  $PbI_2$ ); (d), (e), and (f) are the top surface thermal image of  $T_T$  device, SEM, and XRD at 25 °C for  $S_T$  cases, respectively; (g), (h), and (i) are the top surface thermal image of  $T_T$  device, SEM, and XRD at 45 °C for  $S_T$  cases, respectively (arrow in SEM suggests initiation of intermediate formation leading to the conflation of carbon and  $Al_2O_3$  layer); (j), (k) and (l) are the top surface thermal image of  $T_T$  device, SEM, and XRD at 65 °C for  $S_T$  cases, respectively (arrow in SEM images suggests the zone of  $PbI_2$  exfoliation and conflation of layers).

On increasing the temperatures from 25 °C, major variations of thermal profiles on different layers were not significantly observed at 45 °C for  $T_T$  devices. Analysing  $S_T$  devices at 45 °C, the minimal defects in both the SEM and XRD have been depicted, as shown in Fig. 3h and 3i, respectively. At 45 °C, the formation of low intense intermediate phases as observed from corresponding XRD study further indicates conflation of carbon and m- $Al_2O_3$  layers as observed from the SEM image (Fig. 3h). Stepping up for much higher temperature from 45 °C to 65 °C, the pattern observed (Fig. 3j-l) was similar to that of the low temperature one for  $S_T$  devices. The thermal image of the  $T_T$  testing device at 65 °C indicates a relatively higher temperature of m- $TiO_2$  and m- $Al_2O_3$  than the carbon layer, which clarifies faster ion migration within those layers as observed at the low temperature.<sup>21</sup> The thermal images were reversible as lowering of temperature made a similar trend for  $T_T$  testing. The SEM image at 65 °C signifies the factor responsible for the emergence of an interstitial layer of  $S_T$  devices, Fig. 3k. This *in-situ* layer exfoliates through other layers leading to degrading the device performance. This may be due to the formation of an *in-situ* intermediate structure in the interstitial position affecting the temperature transfer process, which can be confirmed by further characterizations. Regarding  $T_T$  devices, it is interesting to notice that for all the temperature variation cases, the carbon layer possesses a relatively perceptible temperature compared to other layers of the concerned device. The effect of heating from the bottom surface, i.e. from glass/FTO surface is therefore interpreted an essential factor as the device is not influenced by any other external factors such as light, moistures. Fundamentally, thermal conductivity dictates the effective transfer of heat, and as the top layer, the carbon suffers from less heating at an instant. Besides, carbon electrode has graphite in a large amount, and the previous reports say that graphite has a low thermal conductivity at the high-temperature region.<sup>53</sup> Also, the role of specific heat capacities of materials is highly significant to maintain the temperature of the layers. From



available data, it was found that the specific heat capacities of other layers are lower than that of the carbon layer (having carbon black and graphite mainly) which produce this kind of behaviour.<sup>54–56</sup>



**Fig. 4** (a), (b), (c), and (d) are the SEM images of  $S_T$  testing devices at 15 °C, 35 °C, 55 °C, and 75 °C respectively. Energy dispersive X-ray (EDX) elemental colour mapping of Ti, Al, Pb, and I of the devices at 5 °C, 25 °C, and 65 °C.

It can be one more potential reason behind this kind of thermal imaging response. Again, at the very low-temperature surrounding, the temperature dissipates much slowly from carbon material, as shown in Fig. 3. The lower thermal conductivity of other layers along with specific heat capacity of carbon electrode could be the reason behind this kind of significant physico-

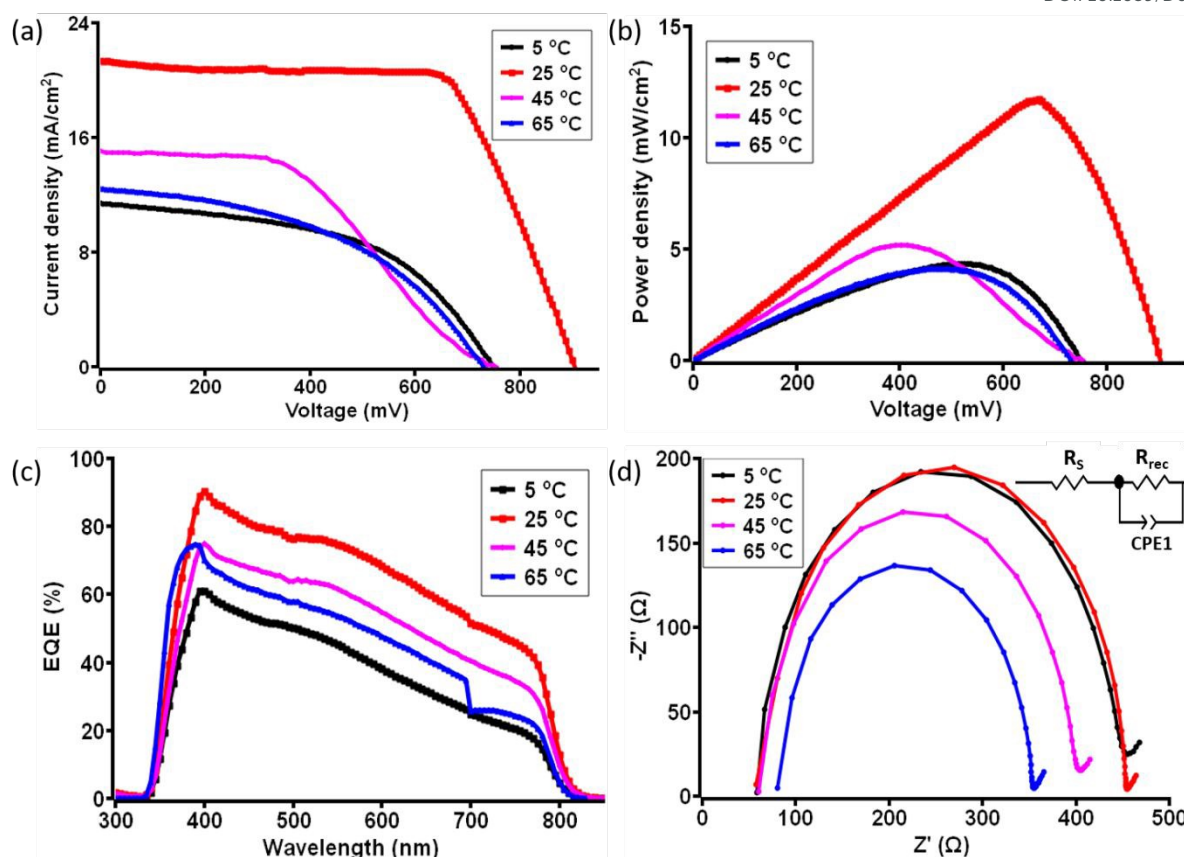


chemical response at low temperature. Materials with higher specific heat capacity have to lose a higher amount of heat energy to change its temperature during the cooling effect, which can be the primary reason for the low-temperature behaviour of carbon electrode.<sup>57</sup> Further study of other intermediate temperature states of  $S_T$  devices has been shown in Fig. 4. The SEM of  $S_T$  devices at 15 °C, 35 °C, 55 °C and 75 °C illustrates the effect of temperature on the microstructural behaviour of the devices. The conflation of layers can be seen clearly at 55 °C, and at the same time, a significant amount of degradation can be observed at very high temperature. The spill-over of degraded material was observed in the FTO coating at 75 °C. The corresponding energy dispersive X-ray (EDX) elemental colour mapping images indicates the extent of the Pb and I formation followed by its proliferation across the different layers of the devices, as shown in Fig. 4

### Photovoltaic performance of c-PSCs for $S_T$ and $T_T$ conditions

In order to understand the correlation of material characterization data and photovoltaic parameter aspect of c-PSC devices regarding their real-world performances, the photovoltaic parameters were prudently monitored for both the  $S_T$  and  $T_T$  devices in the temperature window of 5 °C to 75 °C. For evaluating the performance of the as-prepared c-PSCs made in ambient conditions, the current density vs voltage ( $J-V$ ) characteristics measurements were performed under 1 SUN AM 1.5 (100 mW.cm<sup>-2</sup>) in the temperature range of 5 °C to 75 °C with an increment of 10 °C considered as  $S_T$  condition. The recorded  $J-V$  characteristics parameters are further compared in Table 1. Interestingly, starting from 5 to 25 °C there was a steady increase in the device's PCE, followed by a maximum PCE achieved as 13.1% at 25 °C. After that, a decline of PCE was noticed up to 40 °C, and from 45 to 75 °C, the PCE dropped down extensively. Poor performance at higher temperatures is expected due to the degradation of MAPbI<sub>3</sub>, but the initiation of degradation and its impression on the different layers are still uncovered and need to be addressed.<sup>28,29</sup> Fig. 5a, and Fig. 5b describes the major  $J-V$  characteristics and power density plots at four significant temperatures of the  $S_T$  devices, respectively. Whereas, the overall  $J-V$  characteristics plot recorded for  $S_T$  variations has been shown in Fig. S1a and S1b, ESI. The variation of photovoltaic performances was measured for a set of five devices at each temperature, as shown in Fig. S2, ESI.





**Fig. 5** (a) Current density-voltage ( $J-V$ ) curves and (b) power density-voltage curve for the  $S_T$  PSCs at different temperatures in the range of 5 °C to 75 °C, (c) IPCE spectra of c-PSCs at different temperatures, and (d) corresponding EIS characteristics (Nyquist plots) with the fitted circuit diagram for  $S_T$  devices having the best performance.

Besides, the external quantum efficiency (EQE) curves for c-PSCs exhibited a broad peak over the range of 300-800 nm with a maximum value of  $\sim 90\%$  for devices at 25 °C at a wavelength of 450 nm showing high charge collection efficiency in devices as shown in Fig. 5c and S1(c), ESI. It has been observed that the EQE values are relatively lesser at a lower or higher temperature compared to 25 °C. Higher values of EQE signifies higher charge carrier collection for the solar cell and slow charge recombination process.<sup>58</sup> Further, the calculation of the integrated  $J_{\text{SC}}$  for samples at different temperatures was evaluated from the overlap integral of the IPCE spectra, and values are given in Table S1, ESI. The average integrated  $J_{\text{SC}}$  values of c-PSCs at different temperatures are almost similar to the  $J_{\text{SC}}$  values obtained from the  $J-V$  analysis.





Further, measuring electrochemical impedance spectroscopy (EIS) studies encourage to understand the transport properties at different interfaces of layers in the  $S_T$  c-PSC device. The Nyquist plot with an equivalent circuit diagram of the concerned c-PSCs was recorded under dark at 0.8 V bias from 10 mHz to 1 MHz, as shown in Fig. 5d and S1d, ESI. In the circuit diagram (inset of Fig. 5d),  $R_S$  represents the series resistance, which includes the resistance of FTO and carbon counter electrode.  $R_{rec}$  is charge transfer resistance at the perovskite/carbon interface.<sup>59</sup> In Fig. 5d, the large parabola in the high-frequency region implies higher transportation and exchange resistance from perovskite to carbon counter electrode, which will influence the fill factor as reflected from  $J-V$  characterization. Again, higher values of  $R_S$  should diminish the efficiency, and depending on temperature change  $R_S$  values can be observed from Table S1, ESI.

**Table 1** Photovoltaic parameters of  $S_T$  c-PSC under 1 SUN 1.5G AM (active area of 0.12 cm<sup>2</sup>).

Temperature (°C)	$J_{sc}$ (mA.cm <sup>-2</sup> )	$V_{oc}$ (mV)	FF	PCE <sub>max</sub> (%)	Power <sub>max</sub> (mW.cm <sup>-2</sup> )
5	11.42	752.6	0.51	4.34	4.32
15	16.64	758.8	0.65	8.34	7.84
25	21.34	905.1	0.68	12.0	13.11
35	20.12	902.1	0.54	9.7	9.62
45	15.30	759.2	0.48	5.50	5.15
55	15.16	748.6	0.45	5.14	4.93
65	12.43	734.7	0.45	4.10	4.15
75	12.32	740.3	0.42	3.87	3.76

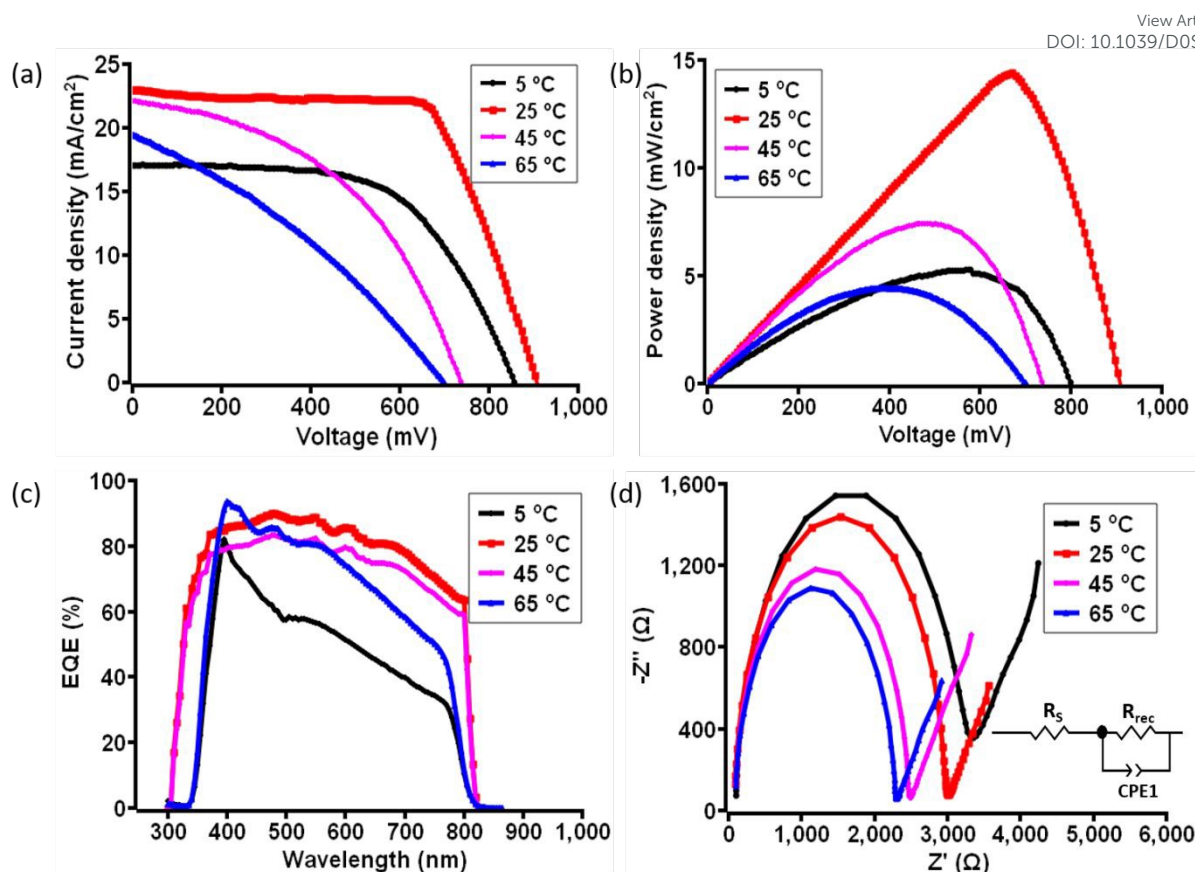
Despite the  $S_T$  observation, a c-PSC device can experience a wide range of temperature. In order to understand the instantaneous behaviour of the photovoltaic performance, a c-PSC device was further employed for  $T_T$  testing. In this case, the performance of the c-PSC devices was also examined in the same way in the temperature range of 5 to 75 °C with an increment of 5 °C. Similarly, the temperature was allowed to decrease from 75 to 5 °C and recorded the data at an interval of every 5 °C. The overall tuning of the temperature window was repeated





twice on the same c-PSC device. The obtained reversible nature of parameters of the champion device is given in supporting information (Fig. S5, ESI). It has been observed that the PCE reduction encountered by  $\sim 10\%$  during the transition of high to low temperature. However, the PCE regained almost its initial values when they were heated back from low temperature. This particular behaviour signifies a negligible effect on the  $T_C$ . The maximum PCE of 14.4% was observed at 25 °C (Fig. 6a), and then a consistent decrease in PCE was reflected during stepping up or stepping down to higher and lower temperatures, respectively. Fig. 6a and 6b describe the major  $J-V$  characteristics and power density plots at four significant temperatures of the  $T_T$  devices, respectively. The performance of all other temperatures is given in Fig. S3a and S3b, ESI. The continuous temperature change may have triggered some internal modifications in the devices, which can be responsible for this phenomenon behaviour. The variation of performances was measured for a set of five devices at each temperature, as shown in Fig. S4, ESI. EQE data of  $T_T$  c-PSCs exhibited a broad peak over the range of 300-800 nm with a maximum value of  $\sim 90\%$  for the device at 25 °C at a wavelength of 450 nm indicating a higher rate of charge collection efficiency in devices as shown in Fig. 6c and S3c, ESI. From the overlap integral of the IPCE spectra, integrated  $J_{SC}$  values were evaluated, and values are mentioned in Table S2, ESI. Besides, the corresponding EIS measurements of  $T_T$  devices are shown in Fig. 6d and S3d, ESI, which reflects a similar nature of data obtained from  $J-V$  characterization. The  $R_S$ ,  $R_{rec}$  values, as recorded from EIS analysis, are mentioned in Table S2, ESI. The photovoltaic performance for both  $S_T$  and  $T_T$  conditions are the influence of interface passivation on the operating temperature of PSCs. The energy barrier, the defects or charge or ion accumulation at perovskite-transport materials interfaces, ions in perovskite or charge transport layers, and charge mobility in charge transport layers determine not only the charge collection efficiency but also have a significant impact on the hysteresis.<sup>60</sup> Though the interfacial layers avoid the direct contact of perovskite film with metal electrodes, the inherent mobile iodide ions in perovskite film can easily diffuse across the interfacial materials to react with the electrode due to the minimal activation energy for their migration.





**Fig. 6** (a) Current density - voltage curves and (b) power density - voltage curve for the best  $T_T$  c-PSC at different temperatures in the range of 5 to 75 °C. Photovoltaic characterization of the best  $T_T$  device for each temperature in the range of 5 °C to 75 °C, (c) IPCE spectra of c-PSCs at different temperatures, and (d) corresponding EIS characteristics (Nyquist plots) with the fitted circuit diagram for  $T_T$  device having the best performance.

**Table 2** Photovoltaic parameters of  $T_T$  c-PSC under 1 SUN 1.5G AM (active area of 0.12 cm<sup>2</sup>).

Temperature (°C)	$J_{sc}$ (mA.cm <sup>-2</sup> )	$V_{oc}$ (mV)	FF	$PCE_{max}$ (%)	$Power_{max}$ (mW.cm <sup>-2</sup> )
5	17.0	860.0	0.59	8.62	8.65
10	17.74	891.4	0.60	9.44	9.38
15	19.69	895.3	0.65	11.30	11.1
20	22.0	894.5	0.68	13.57	12.94
25	23.0	915.0	0.69	14.50	14.43
30	23.36	872.1	0.66	13.40	13.14
35	24.06	835.8	0.55	11.06	11.02



40	22.82	805.9	0.54	9.80	9.54
45	22.13	742.0	0.45	7.47	7.35
50	21.79	768.4	0.44	7.36	7.37
55	20.92	746.1	0.42	6.54	6.48
60	21.45	758.3	0.40	6.44	6.25
65	19.49	703.5	0.33	4.48	4.38
70	18.37	736.2	0.33	4.51	4.48
75	17.34	679.9	0.33	3.80	3.57

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DOI: 10.1039/D0SE00782J

### Evaluation of $T_C$ from the $S_T$ and $T_T$ tested devices

The temperature coefficients quite delineate the behaviour of the c-PSCs photovoltaic parameter function of the temperature. Determination of temperature coefficient ( $T_C$ ) of these two types of testing for c-PSC devices applying the generalized linear relation becomes very much essential for better understanding of temperature-performance correlation in real-world condition as mentioned in the following equations (i) – (iv)<sup>34,41</sup>

$$J_{TC} = (\Delta J / \Delta T) 1/J_{ref} \quad (i)$$

$$V_{TC} = (\Delta V / \Delta T) 1/V_{ref} \quad (ii)$$

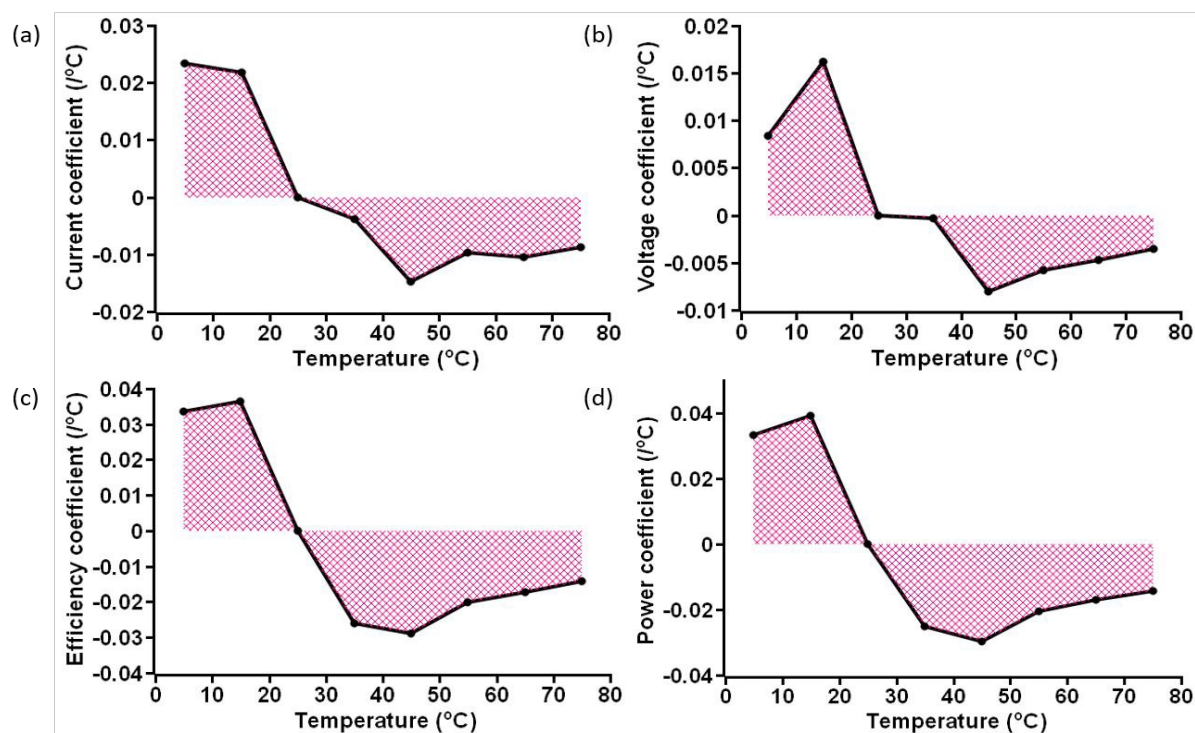
$$\eta_{TC} = (\Delta \eta / \Delta T) 1/\eta_{ref} \quad (iii)$$

$$P_{TC} = (\Delta P / \Delta T) 1/P_{ref} \quad (iv)$$

where,  $J_{TC}$  is the temperature coefficient of current density,  $\Delta J$  is the difference of short-circuit current density at a particular temperature concerning reference temperature (reference temperature is 25°C),  $J_{ref}$  is current density at the reference temperature,  $V_{TC}$  is the temperature coefficient of open-circuit voltage,  $\Delta V$  is the difference of open-circuit voltage at a particular temperature concerning the reference temperature,  $V_{ref}$  is the open-circuit voltage at the reference temperature,  $\eta_{TC}$  is the efficiency temperature coefficient (ETC) / °C,  $\Delta \eta$  is the difference of efficiency at a particular temperature concerning the reference temperature,  $\eta_{ref}$  is the efficiency at the reference temperature,  $P_{TC}$  is the temperature coefficient of power density,  $\Delta P$  is the difference of power density at a particular temperature with respect to the reference temperature,  $P_{ref}$  is the power density at the reference temperature, and  $\Delta T$  is the temperature difference between device temperature and reference temperature. Using equations (1), (2), (3) and, (4) quite a remarkable trend was obtained in the TC values for  $S_T$  and  $T_T$  processes.

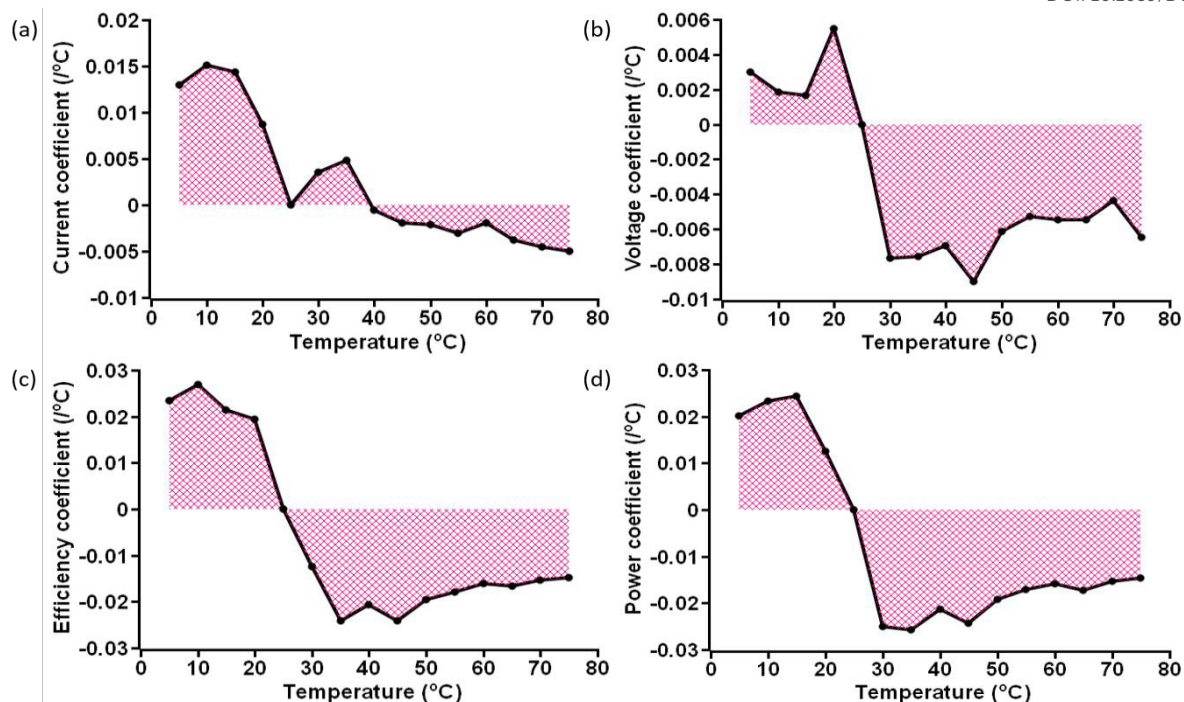


The variation of obtained  $T_C$  values at concerning temperature are shown in Fig. 7 and Fig. 8, for  $S_T$  and  $T_T$  methods, respectively. Clear distinction of the average  $T_C$  values is acquired for  $S_T$  and  $T_T$  processes, as shown in Table 3. The average  $T_C$  values of current density for  $S_T$  and  $T_T$  conditions have significant discrimination from each other. In the case of the  $T_T$  process, the current density increases from 5 to 35°C, but for  $S_T$  testing, the increase occurs up to 25°C.  $T_C$  values of other parameters for two different scenarios seem to be close. However, these variations lead to significant differences in the PCE and other parameters of devices at two different testing conditions, as shown in Table 1 and 2. Also, the conditions are entirely different in these two testing states, which makes  $T_C$  values more significant. Moreover, the  $T_C$  values resulting from  $T_T$  testing conditions are reversible, whereas  $S_T$  testing devices do not show such behaviour, and hence resulting in faster degradation.



**Fig. 7** Area plot of the variation of (a) current coefficient, (b) voltage coefficient, (c) efficiency coefficient, and (d) power coefficient at concerning temperatures for  $S_T$  devices.





**Fig. 8** Area plot of the variation of (a) current coefficient, (b) voltage coefficient, (c) efficiency coefficient, and (d) power coefficient at concerning temperatures for  $T_T$  devices.

<b>Table 3</b> Average values of temperature coefficients for $S_T$ and $T_T$ testing devices at different temperature range. (NA: not applicable)				
Temperature (T) range (°C)	Average temperature coefficient of $J_{SC}$ ( $\times 10^{-2}$ )	Average temperature coefficient of $V_{OC}$ ( $\times 10^{-2}$ )	Average temperature coefficient of $PCE_{max}$ ( $\times 10^{-2}$ )	Average temperature coefficient of Power density $_{max}$ ( $\times 10^{-2}$ )
<b><math>S_T</math> testing</b>				
$5 \leq T \leq 25$	+2.3	+1.2	+3.5	+3.6
$25 \leq T \leq 75$	-0.9	-0.4	-2.1	-2.2
<b><math>T_T</math> testing</b>				
$5 \leq T \leq 25$	+1.2	+0.3	+2.5	+2.0
$25 \leq T \leq 35$	+0.4	N	NA	NA
$35 \leq T \leq 75$	-0.3	NA	NA	NA
$25 \leq T \leq 75$	NA	-0.6	-1.8	-1.9

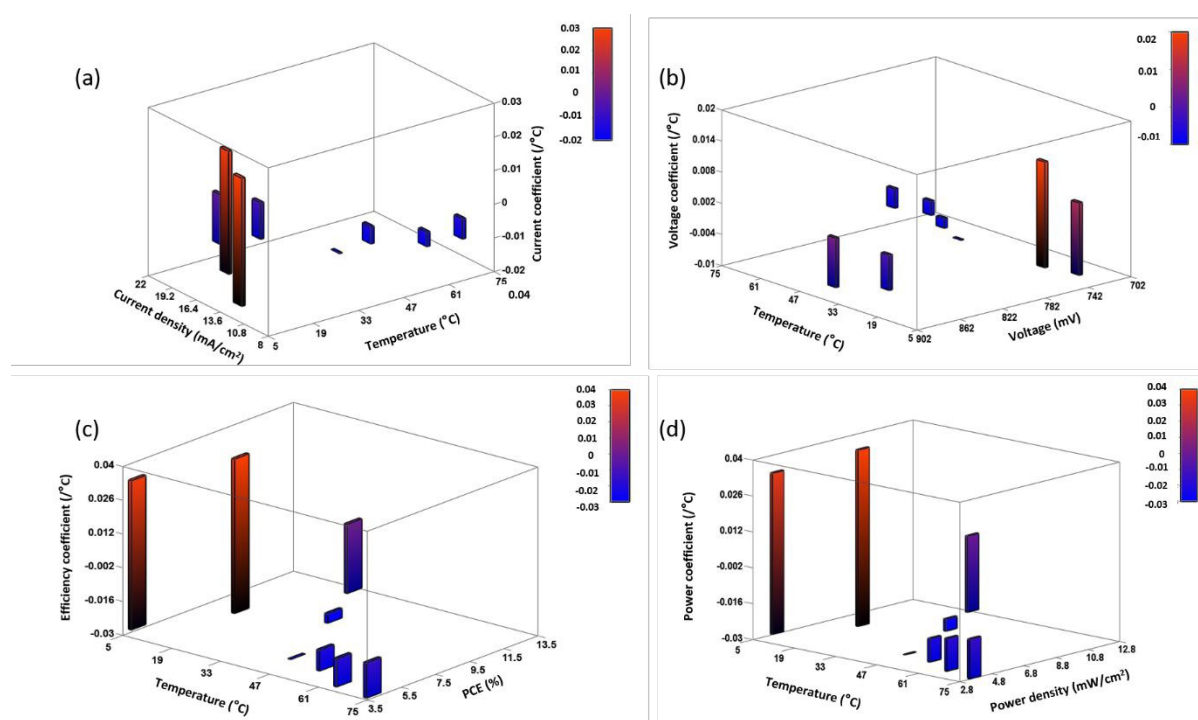
Besides, the temperature-dependent  $T_C$  excels interesting features concerning various photovoltaic parameters, and temperatures as shown as three-dimensional (3D) representation





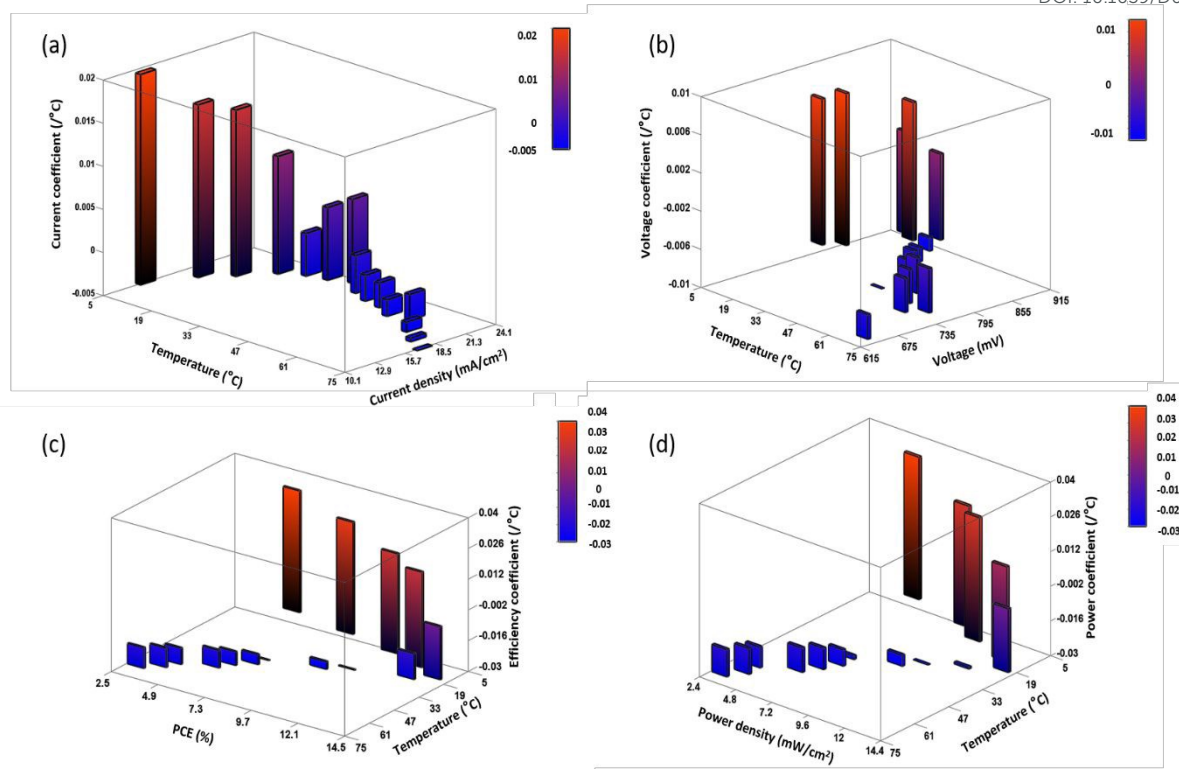
plots in Fig. 9 and Fig. 10. The figures dictate a similarity in  $T_C$  as reported for other traditional solar cells only in the high-temperature region (negative  $T_C$ ) but not at temperatures below STC (positive  $T_C$  for c-PSC), which can make them a more front runner for commercialization.<sup>22</sup> The difference in  $T_C$  plots of  $S_T$  and  $T_T$  testing is fascinating as well for real-world performance analysis.

During the  $T_T$  testing (Fig. 8), the stabilized  $T_C$  values manifest the c-PCSs more realistic in those parts of the world where temperature variation throughout the day is very high. On the other hand,  $S_T$  temperature condition can notably be considered in those parts where the variation of weather in a day is very low throughout a particular season. Moreover, the lower  $T_C$  value for a c-PSC appears as a suitable candidate for a multi-junction solar cell.



**Fig. 9** 3D bar plot of (a) current coefficient, (b) voltage coefficient, (c) efficiency coefficient, and (d) power coefficient at the concerning temperature and corresponding parameters for  $S_T$  devices.





**Fig. 10** 3D bar plot of (a) current coefficient, (b) voltage coefficient, (c) efficiency coefficient, and (d) power coefficient with respect to temperature, and corresponding parameters for  $T_T$  devices.

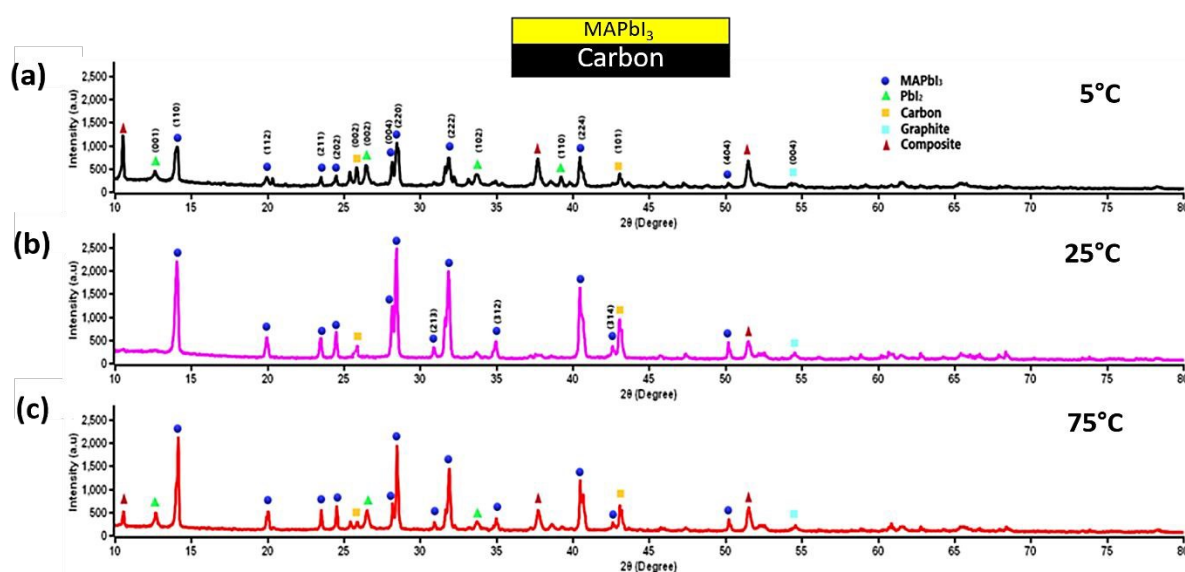
### An overall analysis of c-PSCs at $S_T$ testing condition

It is now highly relevant to realize the variation of  $T_C$  values or rather the performances with in-depth analysis, for which further investigation was executed to recognize the probable origin concerning from the associate layers of the device. The  $\text{MAPbI}_3$  actually controls the device performance, and further its stability.<sup>61</sup> Thus, it is crucial to investigate the role of  $\text{MAPbI}_3$  across the different layers of c-PSC under thermal stress. In order to understand such effect, three different sets of films were prepared on an FTO glass such as (a) spin-coated m- $\text{TiO}_2$ , and  $\text{MAPbI}_3$ ; (b) spin coat m- $\text{Al}_2\text{O}_3$ , and  $\text{MAPbI}_3$ ; (c) screen printing carbon, and spin coating  $\text{MAPbI}_3$ , and applied the  $S_T$  condition.

The XRD pattern at  $5^{\circ}\text{C}$ , and  $65^{\circ}\text{C}$  for  $\text{Al}_2\text{O}_3$  based films exhibit quite distinct characteristics, as shown in Fig. S6, ESI. It has been observed that at the low-temperature appearance of unwanted  $\text{PbI}_2$  is less pronounced compared to the higher temperature. Besides, there is a tendency to cover the  $\text{Al}_2\text{O}_3$  layer by  $\text{PbI}_2$  to some extent, which eases the exfoliation of  $\text{PbI}_2$  formed in the interstitial position. On the other hand, for the m- $\text{TiO}_2$  coated samples, it was



found that the extent of  $\text{PbI}_2$  formation in both high, and low temperatures is quite truncated, as shown in Fig. S7, ESI. Due to lower formation of  $\text{PbI}_2$  weak exfoliation through the  $\text{TiO}_2$  layer is expected. Again, for the carbon-based layer, a substantial amount of information was recognized to understand the low efficiencies at temperatures  $5^\circ\text{C}$ , and  $75^\circ\text{C}$  for the  $\text{S}_\text{T}$  devices. The XRD pattern suggests the formation of an intermediate state by the interaction of carbon and perovskite or degraded perovskite due to thermal treatment, as shown in Fig. 11. This is further leading to more extensive degradation of  $\text{MAPbI}_3$ .

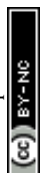


**Fig. 11** XRD data of glass samples coated with  $\text{WO}_3$  doped carbon, and perovskite at  $5^\circ\text{C}$ ,  $25^\circ\text{C}$ , and  $75^\circ\text{C}$ , respectively showing the formation of an intermediate state.

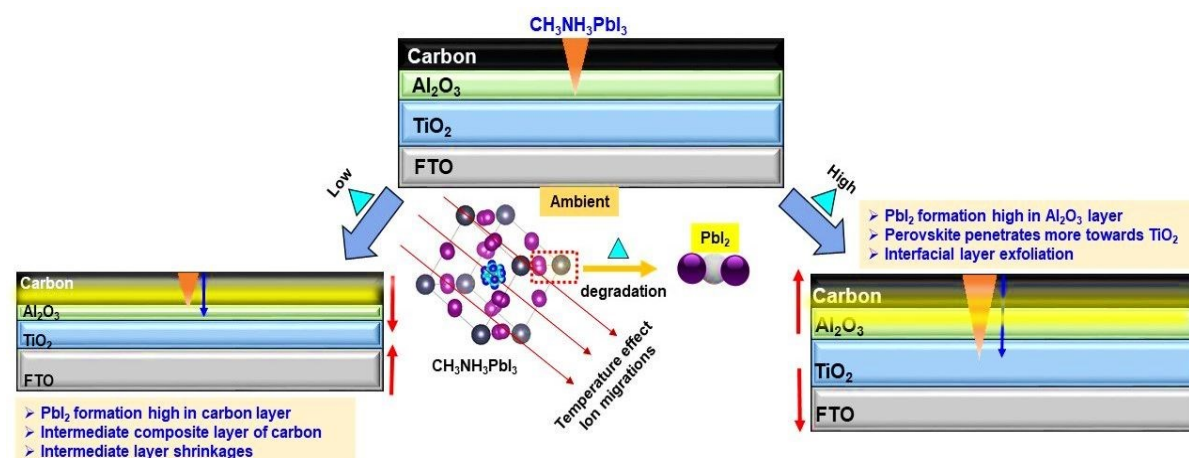
The appearing  $\text{PbI}_2$  phase facilitates increased exfoliation through the layer of the c-PSC. The combination of newly formed unrecognizable intermediate and formation of  $\text{PbI}_2$  severely damages the performances of devices at very high and low-temperature regions. The SEM images also defended the formation of an intermediate phase with carbon, as shown in Fig. S8, ESI. At  $25^\circ\text{C}$ , the SEM (Fig. S8c, ESI) has a prominent surface structure, but dissimilarity can also be observed with temperature variation. On the other hand, the SEM analysis indicates a rapid change occurred at  $15^\circ\text{C}$ , and  $45^\circ\text{C}$  for the  $\text{S}_\text{T}$  devices. The results suggest the initialization of intermediate formation, which points towards the rapid decrease in efficiency at those temperatures. On, the other hand, extrinsic accumulation of  $\text{I}^-$  plays a great role in exfoliation through  $\text{Al}_2\text{O}_3$  and  $\text{TiO}_2$  layers. The extent of degradation is greater when  $\text{MAPbI}_3$  interacts with  $\text{Al}_2\text{O}_3$  rather than  $\text{TiO}_2$ . This elucidates the predominant spill-over of perovskite



through  $\text{Al}_2\text{O}_3$  layer in the  $S_T$  testing devices. The interaction of carbon layer and perovskite greatly influences device performance via the formation of intermediates, and as a whole, the interface of carbon and  $\text{Al}_2\text{O}_3$  is expected to initiate the perovskite deformation. At temperatures above  $45^\circ\text{C}$  and below  $15^\circ\text{C}$  for  $S_T$  testing, creates "pinhole structures", that clearly verifies inter-molecular interaction leading to intermediate formation for devices as shown in SEM (Fig. S8, ESI).<sup>32</sup> The XRD pattern, as shown in Fig. 11, further confirms the formation of such intermediate structures between carbon, and  $\text{MAPbI}_3$  upon exposure to different temperatures for more than a day. The heat produced by high temperature also initiates the chemical decomposition of the  $\text{MAPbI}_3$  film. In this case, the interfacial layers have the direct contact of  $\text{MAPbI}_3$  film with the electrode, the inherent mobile halide ions in the perovskite film can easily diffuse across the interfacial materials to react with the electrode due to the minimal activation energy for their migration. The heat generated at high temperature was also reported to cause migration of metal atoms into PSCs, leading to the degradation of the devices.<sup>61</sup> At the same time, corrosion occurrence from the active carbon and  $\text{Al}_2\text{O}_3$  layer by either the iodide in the perovskite film or the decomposed by-product such as volatile  $\text{I}_2$  and  $\text{HI}$  has also become a significant concern for the high-temperature stress for the operation of the PSC. Temperature stress can able to produce the thermal exfoliation of the layers as observed from different temperature-based SEM analysis, as obtained from Fig. 3. Exfoliation decreases the reachable aperture area of the concerned layers, which accordingly retards the performance of devices. However, the degradation of the device performance of PSCs has also been observed at a lower temperature for  $S_T$  testing. It is observed that at low temperatures the orientation of the methylammonium cation in  $\text{MAPbI}_3$  is fixed because of hydrogen bonding between the  $\text{NH}_3$  groups and the framework iodide atoms. This acts as the driving force for the observed deformation of the  $\text{PbI}_3^-$  framework and further adopting a staggered formation. As the temperature is increased the thermal motion of the cation increases and the  $\text{NH-I}$  interactions weaken.<sup>61</sup> It seems that, in general, the growth of metal oxide might give rise to the lowering of interface quality. It might be related to the presence of surface defect states in metal oxides, which lead to high interface recombination.<sup>62</sup> Also, there will be a slight influence of surrounding moisture and air, although the devices were kept inside a chamber of fixed temperature. It was suggested that excess  $\text{PbI}_2$  in  $\text{MAPbI}_3$  could help to passivate defects at surfaces, and grain boundaries and a small amount of residual  $\text{PbI}_2$  in perovskite supports to reduce charge recombination and improves the  $V_{\text{OC}}$  and  $\text{FF}$ .<sup>59</sup> As a result, the devices do not lose its  $V_{\text{OC}}$  under thermal stress, indicating the PCE loss is mainly restricted with the  $J_{\text{SC}}$ . This kind of materialistic interface dependent performance variation concerning temperature is



highly demanding for real-world application of c-PSC. The discussions mentioned above have been further schematically described in Fig. 12.



**Fig. 12** Schematic view of high, low, and ambient temperature effect on a c-PSC.

### An overall analysis of c-PSCs at $T_T$ testing condition

$T_T$  testing signifies the unique effects of temperature variations on a particular device. The presence of temperature gradient between the layers significantly influenced the performance. The perovskite can become chemically unstable at temperatures well below its decomposition conditions due to temperature gradient.<sup>21</sup> Migration of mobile ions by the influence of temperature stress (majorly iodide ion) is responsible for PSCs unique and prominent properties, although the large-scale trapping of electrons cannot be ruled out.<sup>63–65</sup> Most of the studies suggest, with temperature, mobility of transient ions increases, which leads to the accumulation of ions at interfacial contacts of perovskite, and other layers. As the work function of HTL and ETL differs from each other, this difference creates a built-in field, which drives the migratory ions. Temperature variation can reduce the built-in field, which eventually can increase the extent of ion migration. Thus, the excess mobility of ions leads to accumulation at interfaces. Accumulation of ions reduces current generation due to the increase in the recombination process at interfaces by increasing bandgap defects or electrostatic traps.<sup>66–69</sup> Data obtained from EIS (Fig. 6) confirms high charge recombination resistance pointing towards the hike in the recombination process for the  $T_T$  study. The role of crystal lattice disruption of perovskite (tetragonal to cubic) at a temperature higher than 50 °C cannot be neglected, which significantly reduce the performance of  $T_T$  devices.<sup>70</sup> On the other hand, the thermal expansion coefficients of different materials used can significantly disrupt the interconnectivity of layers, increasing the interfacial defects.<sup>70</sup> The variation of performance at





low temperature may be the result of this expansion factor. Also, the effect of low charge diffusion cannot be neglected at low temperature, which can reduce performance.<sup>71</sup> A correlation between  $S_T$  and  $T_T$  observations can be drawn from this experiment. It is explained earlier intrinsic ion migration and accumulation may be the reason behind performance loss of  $T_T$  devices. Because of thermal stress on the  $T_T$  devices, defect state may occur followed by creating interstitial vacancies.<sup>64</sup> Iodide ion could drift across the interface, and enter in the vacant position. The intermediate formation in  $S_T$  devices could have originated from intrinsic behaviour of  $T_T$  devices. However, the exact nature of the intermediate phase needs clarity leading to research that is more intensive. To the best of our knowledge, we are first to report the  $T_C$  aspect of the carbon-based PSCs. It is anticipated that temperature can significantly influence the photovoltaic parameters of the device. The way of temperature treatment is further indicative of the c-PSCs photovoltaic behaviour, which has been depicted in terms of  $T_C$  for the real-world condition. In this study, we propose that the average  $T_C$  values should closely agree with the observed trend of this study for any c-PSC or rather any PSC. The challenge is the development of advanced high-temperature resistant PSCs, and modules based on novel architectures and/or processes, which can tackle efficiency limitations while improving cost-effectiveness.

## Conclusions

In conclusion, we have investigated the temperature coefficient ( $T_C$ ) of carbon-based perovskite solar cell (c-PSC) in two determining ways such as steady temperature ( $S_T$ ), and transient temperature ( $T_T$ ) conditions across a broad temperature window from 5 to 75 °C. These explorations provide new insights into a PSC in terms of the  $T_C$  analysis based on corresponding different photovoltaic parameters. Highly noticeable performance in short circuit current, open-circuit voltage, fill factor, and power conversion efficiency of the devices concerning temperature was observed, leading to distinct  $T_C$  values separately for the  $S_T$  and  $T_T$  cases. Instantaneous behaviour is pronounced in case of  $T_T$  devices leading to rapid changes happening due to the ion migration and accumulation at interfaces across the c-PSC device. We have observed that the  $T_C$  value becomes higher for  $S_T$  testing devices compared to  $T_T$ , which is further explained by layer interfacial various physicochemical studies. The  $T_C$  values derived from  $T_T$  testing condition are reversible, whereas the irreversible  $T_C$  value of  $S_T$  testing facilitates enduring degradation of the devices. Effect of temperature on the different interfacial layers of the c-PSC and their correlation with the photovoltaic performances have been further



established. The XRD and SEM microstructural analysis further suggested that the extent of perovskite degradation was greater at  $\text{Al}_2\text{O}_3$ -perovskite interface due to the thermal stress. The observed dual characteristics of  $T_C$  for a c-PSC in a low and high-temperature region envisages as a futuristic research interest for its large-scale real-world condition testing. Future studies will be further required to investigate whether other architectures of PSCs or other organo-metal halide perovskites are more robust to the  $T_C$  parameter. The temperature-dependent surface features of the perovskite also highlight the role of the interfacial interaction associated with the different layers in the photovoltaic performance of the solar cells. We assume that further research about the origin of thermal stress on various interfacial layers might help in reducing the photocurrent loss and thereby increasing the likelihood of successful outdoor application of PSCs.

## Materials and Methods

### $\text{CH}_3\text{NH}_3\text{PbI}_3$ synthesis and c-PSC device fabrication

Fabrication of c-PSC was adopted from our earlier reported article with slight modification using the 'crystal growth *via* solvent exchange' (CGSE) method for better performance.<sup>65</sup> In short, sequential deposition of compact  $\text{TiO}_2$  (c- $\text{TiO}_2$ ), mesoporous  $\text{TiO}_2$  (m- $\text{TiO}_2$ ), mesoporous  $\text{Al}_2\text{O}_3$ , and  $\text{WO}_3$  incorporated carbon were performed on fluorine-doped tin oxide (FTO) glass substrate. Perovskite precursor ( $\text{MAPbI}_3$ ) solution was drop-casted, followed by spin coating, and then the CGSE method was deduced following from previous literature.<sup>50</sup> CGSE stand out as an effective one-step approach for the fabrication of organic hole-conductor free carbon-based perovskite solar cells with superior device performance. At the same time, it allows the room-temperature solution processing fabrication method to develop crystalline, scalable, and rapid perovskite thin films with no further heat-treatment. In the CGSE process, coated FTO glasses were immersed in diethyl ether (DEE) bath for 1 hour at room temperature instead of thermal annealing. During the CGSE process, NMP soluble  $\text{MAPbI}_3$  precursor is exposed to DEE, and the NMP solvent is extracted selectively because NMP is highly miscible in DEE. This triggers the crystallization of  $\text{MAPbI}_3$  perovskite in areas devoid of NMP, which spreads rapidly to cover the entire area as NMP is completely extracted by DEE. A schematic diagram has been mentioned, which illustrated about the CGSE process as shown in Fig. 1. The as prepared devices were kept at dry, and dark conditions for three days to obtain a uniform growth of perovskite crystals. Finally, the c-PSCs were employed for further characterization, and measurements. Prepared c-PSC devices were divided into two groups before further



characterization depending on  $S_T$  and  $T_T$  conditions (Fig. 2).  $S_T$  resembles separate devices kept at different temperatures and  $T_T$  indicates a particular device has been tested under variable temperature conditions.  $S_T$  devices were again considered into sub-groups depending on temperature rather in case of  $T_T$  devices, there was no subgroups.

### Material Characterizations

The infra-red (IR) camera shots (thermal images) were taken with a FLIR T425 camera positioned on top of the PSC placed at every different temperature at the base by 10mm. The cross-sectional thickness measurement and elemental mapping of the PSC were recorded on a scanning electron microscope (SEM-EDX), (LEO 430i, Carl Zeiss). X-ray diffraction (XRD) analysis of the fabricated PSC films was carried out on an X'pert pro MPD XRD of PAN analytical with Cu K $\alpha$  radiation ( $\lambda = 1.5406 \text{ \AA}$ ). Further, testing of the PSC was executed under  $1000 \text{ W/m}^2$  of light from a Wacom AAA continuous solar simulator (model: WXS-210S-20, AM1.5G). The  $I$ - $V$  characteristic of the devices was recorded using an EKO MP-160i  $I$ - $V$  Tracer. EIS measurements were carried out with an AUTOLAB frequency analyzer setup equipped with an AUTOLAB PGSTAT 10, and a Frequency Response Analyzer (FRA) Module. The measurements were performed under the same solar simulator condition with the frequency range from 10 mHz to 1 MHz. All the devices were measured at the 0.80 V open-circuit voltage of the devices. The experimental data were fitted with the Z-view software (version 3.4d, Scribner Associates, Inc., USA) using appropriate equivalent circuits. Incident photon to current efficiency (IPCE) was carried out on a BENTHAM PVE300 Photovoltaic EQE (IPCE), and IQE solution under 350-750 nm wavelength using tungsten halogen lamp source.<sup>45</sup> All the data presented are an average of measurements taken on five different devices.

### Conflicts of interest

The authors declare no conflicts of interest.

### Acknowledgement

S.B acknowledges the College of Engineering, Mathematics, and Physical Sciences, the University of Exeter for his PhD fellowship. Partial funding from the EPSRC funded JUICE project (EP/P003605/1) is acknowledged.

### Data availability statements



The data that support the plots within this paper, and other finding of this study are available from the corresponding author upon reasonable request.

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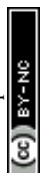
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